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10/797,231	03/10/2004	Richard Hammond	ASC-057C1	2980

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GOODWIN PROCTER LLP
PATENT ADMINISTRATOR
53 STATE STREET
EXCHANGE PLACE
BOSTON, MA 02109-2881

EXAMINER	
GHYKA, ALEXANDER G	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
12/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PatentBos@goodwinprocter.com
hmcpeake@goodwinprocter.com
glenn.williams@goodwinprocter.com

Office Action Summary	Application No.	Applicant(s)	
	10/797,231	HAMMOND ET AL.	
	Examiner	Art Unit	
	ALEXANDER G. GHYKA	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-35,38-54 and 56-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-35,38-54 and 56-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/6/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response of 11/06/2008 has been considered and entered in the record. The following new rejections are made in view of Applicants' amendments. Applicants arguments have been considered, but they are moot in view of the new grounds of rejection. Claims 1-27, 36-37 and 55 are cancelled. Claims 56-73 are added. Claims 28-35, 38-54 and 56 -73 are now under consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 28-35, 38-40, 43 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ismail (Si/SiGe High Speed Field Effect Transistors, IEEE

1995) "Ismail" in view of Chang et al (Selective Etching of SiGe on SiGe/Si Heterostructures, J. Electrochem, Soc. Vol 138, No. 1, 1991 "Chang et al") and Hellberg et al (Oxidation of silicon-germanium alloys. I. An experimental study, J. of Applied Phys. 82 , 1 December 1997, "Hellberg et al") .

The present Claims generally require providing a strained semiconductor layer; providing a SiGe layer over said strained semiconductor layer; and selectively removing said SiGe layer to expose said strained semiconductor layer, wherein selectively removing said SiGe layer comprises thermal oxidation performed at or below a temperature of approximately 850 degrees Celcius.

Ismail et al shows a FET formed providing a strained semiconductor layer; providing a SiGe layer over the strained semiconductor layer. See Figure 7, pg 20.01.03. The strained semiconductor layer comprises Si as required by present Claim 29. A relaxed semiconductor layer comprising Si and Ge is provided beneath the strained layer as required by present Claims 31-33. See Figure 7, page 20.1.3. With respect to Claims 34-35, Ismail discloses an insulator layer and exemplifies silicon dioxide. See last paragraph of column 1, page 20.1.3. With respect to Claims 40 and 43, Ismail discloses MOSFETs. See Figure 9, page 20.1.3.

However, Ismail does not disclose selectively removing the SiGe layer to expose the strained semiconductor layer or thermal oxidation performed at or below a temperature of approximately 850 degrees Celcius .

Chang et al disclose a method for selectively removing SiGe disposed over Si by chemically oxidizing the SiGe to form a SiGe oxide in one region but not in another and then removing the oxidized SiGe. See page 202, columns 1 and 2 and page 203, Fig 4.

Hellberg et al disclose the equivalence of wet and dry oxidation for SiGe surfaces, and disclose temperatures of less than 850 degrees Celcius. See page 5773 columns 1 and 2.

It would be obvious for one of ordinary skill in the art, at the time of the invention, to use the oxidation and etch method of Chang et al, to form the SiGe/Si structures of Ismail, for their known benefit in the art of selectively removing the SiGe layer as disclosed by the Chang et al reference. Moreover, it would have been obvious for one of ordinary skill in the art, at the time of the invention, to use thermal oxidation in the process of Ismail and Chang et al, for its known benefit of oxidizing SiGe surfaces as disclosed by Hellberg et al.

With respect to Claims 38-39, the oxidation and etch technique as required by the afore mentioned Claims, are disclosed by the Chang reference.

With respect to Claims 43 and 45, it would have been obvious to one of ordinary skill in the art to use the MODFET and MOSFET structures on the same substrate, for their respective benefits as disclosed by Ismail et al. Figure 7 of Ismail discloses a buried channel and a surface channel as required by Claim 45.

Claims 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ismail (Si/SiGe High Speed Field Effect Transistors, IEEE 1995) "Ismail" in view of Chang et al (Selective Etching of SiGe on SiGe/Si Heterostructures, J. Electrochem, Soc. Vol 138, No. 1, 1991 "Chang et al") and Hellberg et al (Oxidation of silicon-germanium alloys. I. An experimental study, J. of Applied Phys. 82 , 1 December 1997, "Hellberg et al") as applied to claims 28-35, 38-40, 43 and 45 above, and further in view of Suematsu et al (US 6,044,255) or Sugiyama et al (US 6,191,432).

Ismail, Chang and Hellberg et al are relied upon as discussed above.

The references differ from the afore mentioned Claims in that a MOSFET device is not disclosed in Figure 7 of Ismail, but a MODFET.

Suematsu disclose a radio frequency circuit with integrated elements, and disclose the equivalence of MODFETs and MOSFETs , and the use of SiGe substrates. See column 9, lines 20-45.

Sugiyama et al disclose the equivalence of MODFET and MOSFET devices in memory devices, and the use of SiGe substrates. See column 1, lines 40-60.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to form a MOSFET device in the process of Ismail, Chang and Hellberg et al, instead of a MODFET, as Suematsu et al or Sugiyama et al disclose the equivalence of MODFETs and MOSFETs in certain cases in integrated circuits. The substitution of a MODFET for a MOSFET would therefore have been obvious to one of ordinary skill in the art.

Claims 42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ismail (Si/SiGe High Speed Field Effect Transistors, IEEE 1995) "Ismail" in view of Chang et al (Selective Etching of SiGe on SiGe/Si Heterostructures, J. Electrochem, Soc. Vol 138, No. 1, 1991 "Chang et al"), Hellberg et al (Oxidation of silicon-germanium alloys. I. An experimental study, J. of Applied Phys. 82 , 1 December 1997, "Hellberg et al") and Suematsu et al (US 6,044,255) or Sugiyama et al (US6,191,432), as applied to claims 41 and 43 above, and further in view of Boyd et al (US 6,271,094).

Ismail, Chang et al, Hellberg et al, Suematsu et al and Sugiyama et al are relied upon as discussed above.

However, Ismail, Chang et al, Hellberg et al, Suematsu et al and Sugiyama et al do not disclose the use of a high k insulator in a MOSFET.

Boyd et al disclose a MOSFET which comprises a SIGe layer and the use of a high k dielectric layer. See column 2, lines 5-65 and column 9, lines 55-60.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use a high k dielectric in the MOSFET of Ismail, Chang et al, Hellberg et al, Suematsu et al and Sugiyama, for its known benefit as an insulator in MOSFETs as disclosed by Boyd. The use of a known material, high k dielectric, for its known purpose, an insulator in a MOSFET would be within the skill of one of ordinary skill in the art.

Claims 46-54 and 56-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ismail (Si/SiGe High Speed Field Effect Transistors, IEEE 1995)

"Ismail" in view of Chang et al (Selective Etching of SiGe on SiGe/Si Heterostructures, J. Electrochem, Soc. Vol 138, No. 1, 1991 "Chang et al"), and Suematsu et al (US 6,044,255) or Sugiyama et al (US6,191,432), and further in view of Boyd et al (US 6,271,094).

As discussed above, Ismail et al shows a FET formed providing a strained semiconductor layer; providing a SiGe layer over the strained semiconductor layer. See Figure 7, pg 20.01.03. The strained semiconductor layer comprises Si. A relaxed semiconductor layer comprising Si and Ge is provided beneath the strained layer. See Figure 7, page 20.1.3. Ismail discloses an insulator layer and exemplifies silicon dioxide. See last paragraph of column 1, page 20.1.3. Ismail discloses MOSFETs. See Figure 9, page 20.1.3.

However, Ismail does not disclose selectively removing the SiGe layer to expose the strained semiconductor layer or the equivalence of MODFETS and MOSFETS or the use of a high k dielectric layer in a MOSFET.

Chang et al disclose a method for selectively removing SiGe disposed over Si by chemically oxidizing the SiGe to form a SiGe oxide in one region but not in another and then removing the oxidized SiGe. See page 202, columns 1 and 2 and page 203, Fig 4.

It would be obvious for one of ordinary skill in the art, at the time of the invention, to use the oxidation and etch method of Chang et al, to form the SiGe/Si structures of Ismail, for their known benefit in the art of selectively removing the SiGe layer as disclosed by the Chang et al reference

Suematsu disclose a radio frequency circuit with integrated elements, and disclose the equivalence of MODFETs and MOSFETs , and the use of SiGe substrates. See column 9, lines 20-45.

Sugiyama et al disclose the equivalence of MODFET and MOSFET devices in memory devices, and the use of SiGe substrates. See column 1, lines 40-60.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to form a MOSFET device in the process of Ismail (Figure 7) and Chang et al, instead of a MODFET, as Suematsu et al or Sugiyama et al disclose the equivalence of MODFETs and MOSFETs in certain cases in integrated circuits. The substitution of a MODFET for a MOSFET would therefore have been obvious to one of ordinary skill in the art.

Boyd et al disclose a MOSFET which comprises a SIGe layer and the use of a high k dielectric layer. See column 2, lines 5-65 and column 9, lines 55-60.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use a high k dielectric in the MOSFET of Ismail and Chang et al, Suematsu et al and Sugiyama, for its known benefit as an insulator in MOSFETs as disclosed by Boyd. The use of a known material, high k dielectric, for its known purpose, an insulator in a MOSFET would be within the skill of one of ordinary skill in the art.

With respect to Claims 47-54, Ismail et al Figures 7 and 8 disclosed source and drain regions, the respective doping, and the strained and relaxed SiGe layers as required by the present Claims

With respect to Claim 56 and 58, the use of a MOSFET in Figure 7 of Ismail, for the reasons as discussed above would read on the limitation forming a MOSFET in the first region or the second region.

With respect to Cllaim 57 and 59, Boyd et al disclose a high k dielectric as discussed above.

With respect to Claims 60-73, Ismail et al Figures 7 and 8 disclosed source and drain regions, the respective doping, and the strained and relaxed SiGe layers as required by the present Claims

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Friday during general business hours. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 14, 2008
AGG

ALEXANDER G. GHYKA

PRIMARY EXAMINER AU 2812

/Alexander G. Ghyka/